Burr-Brown Products
from Texas Instruments

VECANA01

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10-Channel, 12-Bit DATA ACQUISITION SYSTEM

FEATURES

- 10 FULLY DIFFERENTIAL INPUTS
- 5 SIMULTANEOUS SAMPLED CHANNELS PLUS 2 SYNCHRONIZED SAMPLING CHANNELS
- 3 SYNCHRONIZED 12-BIT ADCs
- 12.8μs THROUGHPUT RATE
- DIGITALLY SELECTABLE INPUT RANGES
- ±5V POWER SUPPLIES
- SERIAL DIGITAL INPUT/OUTPUTS
- 7 SIGN AND 3 DIGITALLY PROGRAMMABLE WINDOW COMPARATOR

APPLICATIONS

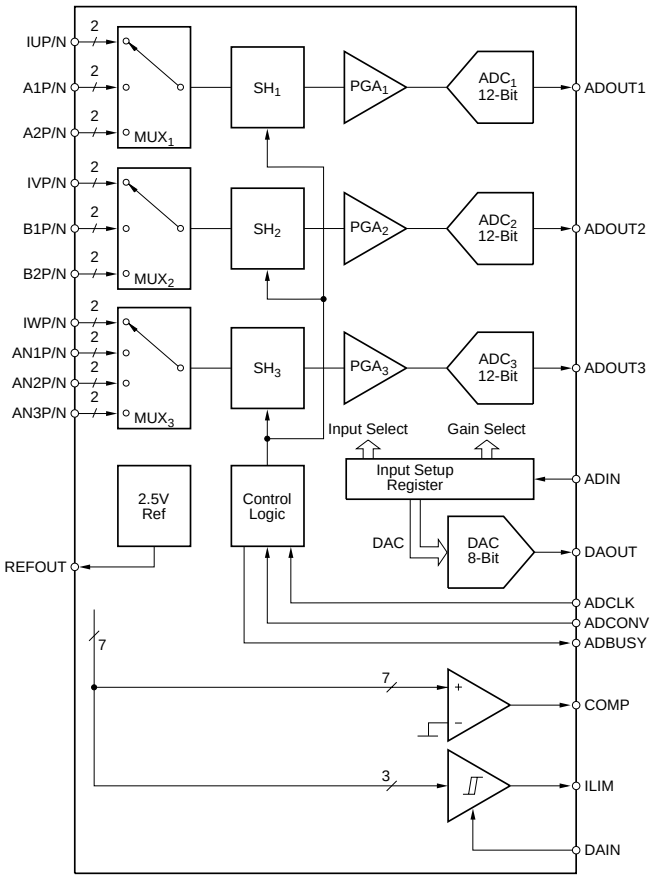
- AC MOTOR SPEED CONTROLS
- THREE PHASE POWER CONTROL
- UNINTERRUPTABLE POWER SUPPLIES
- VIBRATION ANALYSIS

DESCRIPTION

The VECANA01 consists of three 12-bit analog-to-digital converters preceded by five simultaneously operating sample-hold amplifiers, and multiplexers for 10 differential inputs. The ADCs have simultaneous serial outputs for high speed data transfer and data processing.

The VECANA01 also offers a programmable gain amplifier with programmable gains of 1.0V/V, 1.25V/V, 2.5V/V, and 5.0V/V. Channel selection and gain selection are selectable through the serial input control word. The high through put rate is maintained by simultaneously clocking in the 13-bit input control word for the next conversion while the present conversions are clocked out.

The part also contains an 8-bit digital-to-analog converter whose digital input is supplied as part of the input control word.



TEXAS INSTRUMENTS

SBAS155

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SPECIFICATIONS

At V_{ANA+} = +5V, V_{ANA-} = –5V, V_{DIG+} = +5V, V_{DIG-} = –5V, and T_A = –40°C to +85°C, using internal reference, f_{CLOCK} = 1.25MHz.

ANALOG-TO-DIGITAL CONVERTER CHANNELS

PARAMETER	CONDITIONS	VECANA01N MIN	VECANA01N TYP	VECANA01N MAX	UNITS
RESOLUTION		12			Bit
ANALOG INPUT					
Full Scale Voltage, Differential	G = 1.0V/V		±2.5		V
	G = 1.25V/V		±2.0		V
	G = 2.5V/V		±1.0		V
	G = 5.0V/V		±0.5		V
Common-Mode Voltage		±0.5	See Table VII		V
Impedance			10^{12}		Ω
Capacitance			20		pF
THROUGHPUT SPEED					
Conversion Time	CLK = 1.25MHz			10.4	µs
Complete Cycle	Acquire and Convert			12.8	µs
Throughput Rate		78			kHz
SAMPLING DYNAMICS					
S/H Droop Rate			0.1		µV/µs
S/H Acquisition Time			0.5		µs
S/H Aperture Delay			50		ns
S/H Aperture Jitter			50		ps
Sampling Skew, Channel-to-Channel			3		ns
DC ACCURACY					
Integral Linearity - ADC			±0.5	±2	LSB
Differential Linearity - ADC			±0.5	±2	LSB
No Missing Codes		12			Bits
Integral Linearity - Asynchronous, Synchronous			0.5	±3	LSB
Differential Linearity - Asynchronous, Synchronous			0.5	±3	LSB
Full Scale Error	G = 1.0V/V			2	% of FSR
Full Scale Error Other Gains				4	% of FSR
Full Scale Error Drift	G = 1.0V/V		±10	±100	ppm/°C
	G = 2.5V/V		±10	±100	ppm/°C
Zero Error - ADC	G = 1.0V/V		±0.5	±15	LSB
Zero Error - Asynchronous, Synchronous	G = 1.0V/V		±0.5	±20	LSB
Zero Error Drift	G = 1.0V/V		±0.5		ppm/°C
AC ACCURACY					
Total Harmonic Distortion					
f_{IN} = 1kHz			92		dB
f_{IN} = 1MHz			70		dB
CMR	V_{CM} = ±0.5V, f_{CM} = 1MHz		50		dB
REFERENCE					
Internal Reference Voltage			2.5		V
Internal Reference Accuracy			±0.25	±2	%
Internal Reference Drift			±10		ppm/°C
Internal Reference Source Current			10		µA
External Reference Voltage Range for Specified Linearity		2.25	2.5	2.75	V
External Reference Current Drain			10		µA
DIGITAL INPUTS					
Logic Levels					
V_{IL}		0		1.5	V
V_{IH}		+3.5		+5	V
I_{IL}				±10	µA
I_{IH}				±10	µA
Input Capacitance	At All Digital Input Pins			15	pF
DIGITAL OUTPUTS					
Data Format			12-Bit Serial		
Data Coding			BTC		
V_{OL}	I_{SINK} = 1.6mA	0		0.4	V
V_{OH}	I_{SOURCE} = 500µA	4.2		5	V
Leakage Current				±5	µA
Output Capacitance	At All Digital Output Pins			15	pF

SPECIFICATIONS (Cont.)

At V_{ANA+} = +5V, V_{ANA-} = –5V, V_{DIG+} = +5V, V_{DIG-} = –5V, and T_A = –40°C to +85°C, using internal reference, f_{CLOCK} = 1.25MHz.

ANALOG-TO-DIGITAL CONVERTER CHANNELS

PARAMETER	CONDITIONS	VECANA01N MIN	VECANA01N TYP	VECANA01N MAX	UNITS
POWER SUPPLIES	Specified Performance				
V_{ANA+}		+4.75	+5.0	+5.25	V
V_{ANA-}		–4.75	–5.0	–5.25	V
V_{DIG+}		+4.75	+5.0	+5.25	V
V_{DIG-}		–4.75	–5.0	–5.25	V
I_{ANA+}			15		mA
I_{ANA-}			–8		mA
I_{DIG+}			12		mA
I_{DIG-}			–10		mA
Power Dissipation			225		mW
TEMPERATURE RANGE					
Specified Performance		–40		+85	°C
Derated Performance		–55		+125	°C
Storage		–65		+150	°C

DIGITAL-TO-ANALOG CONVERTER

PARAMETER	CONDITIONS	VECANA01N MIN	VECANA01N TYP	VECANA01N MAX	UNITS
RESOLUTION		8-Bits			
Output Range		0		+2.5	V
Output Settling Time	0.5LSB		0.2	1	µs
Linearity Error				±1	LSB
Differential Linearity				±1	LSB
Output Current		200			µA
Offset Error			±1	±10	mV
Full Scale Error (including REF)				±2	%

SIGN AND WINDOW COMPARATORS

PARAMETER	CONDITIONS	VECANA01 MIN	VECANA01 TYP	VECANA01 MAX	UNITS
Differential Input Voltage Range of the Window Comparators				±2.5	V
Offset Error of the Window Comparators			±20	±80	mV
Hysteresis of the Window Comparators			60	100	mV
Offset Error of the Sign Current Comparators			±5	±20	mV
Hysteresis of the Sign Current Comparators			10	30	mV
Offset Error of the Sign Sensor Signal Comparators			±5	±30	mV
Hysteresis of the Sign Sensor Signal Comparators			75	90	mV
Absolute Input Range of the Comparators			±2.9	±3.2	V
Delay Time of the Sign Comparators			25	150	ns
Delay Time of the Window Comparators			250	1500	ns

ABSOLUTE MAXIMUM RATINGS

Ground Voltage Difference: AGND and DGND ..... ±0.3V
Power Supply Voltages:
V_{ANA+} ..... +7V
V_{ANA-} ..... –7V
V_{DIG+} ..... +7V
V_{DIG-} ..... –7V
Digital Inputs ..... –0.3V to V_{DIG} +0.3V
Maximum Junction Temperature ..... +165°C
Internal Power Dissipation 825mW
Lead Temperature (soldering, 10s) ..... +300°C

CONVERSION AND DATA TIMING

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{CONV}	A/D Conversion Time	10.4	6.2		µs
CLK	A/D Conversion Clock	1.25	2.1		MHz
t_1	Setup Time for Conversion Before Rising Edge of Clock	50			ns
t_2	Hold Time for Conversion After Rising Edge of Clock	50			ns
t_3	Setup Time for Serial Out		125		ns
t_4	Setup Time for Serial Input	30			ns
t_5	Hold Time for Serial Input	30			ns

ELECTROSTATIC DISCHARGE SENSITIVITY

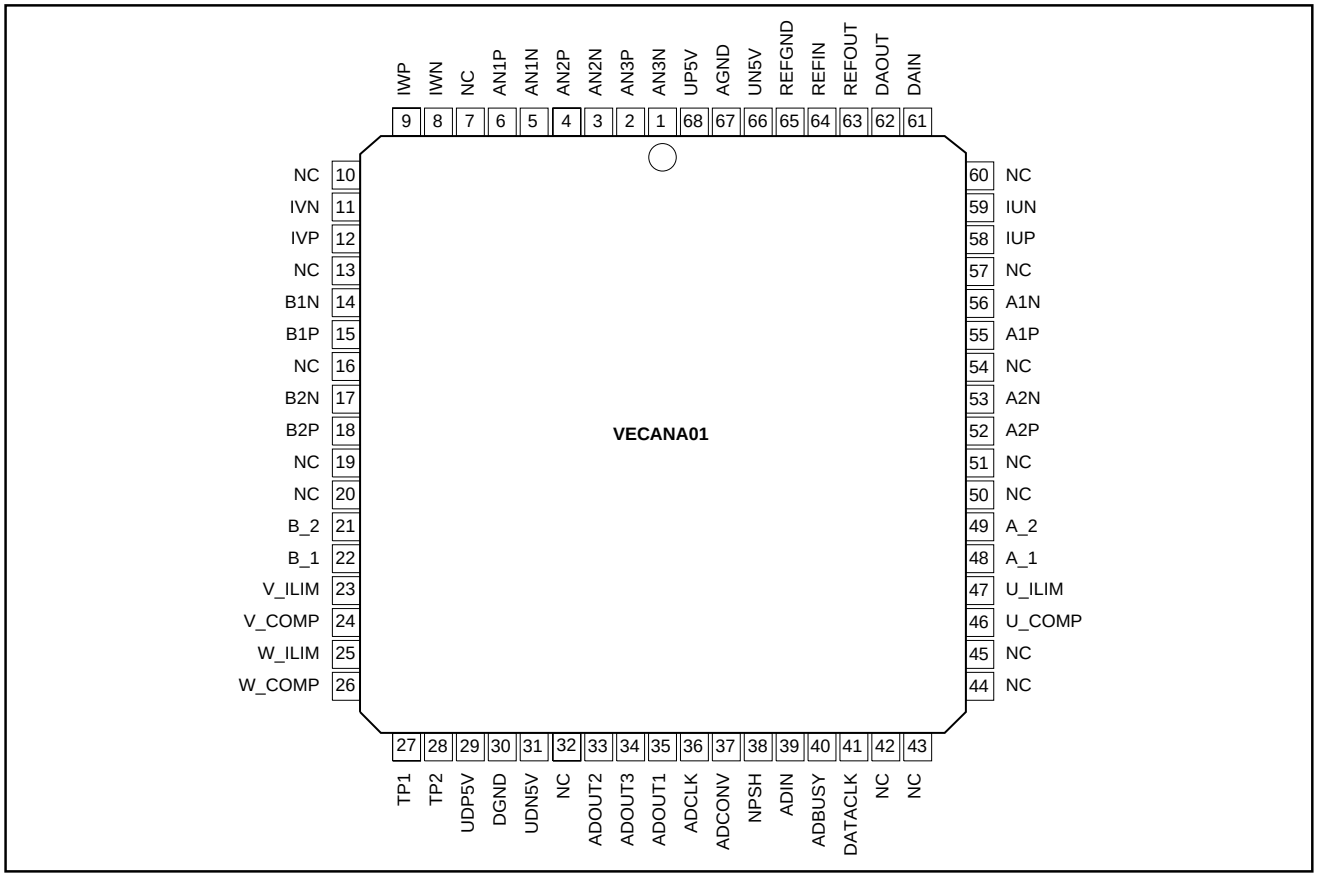
This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA
VECANA01	PLCC-68	312	–40°C to +85°C	VECANA01	VECANA01	Rails

PIN CONFIGURATION



PIN DEFINITIONS

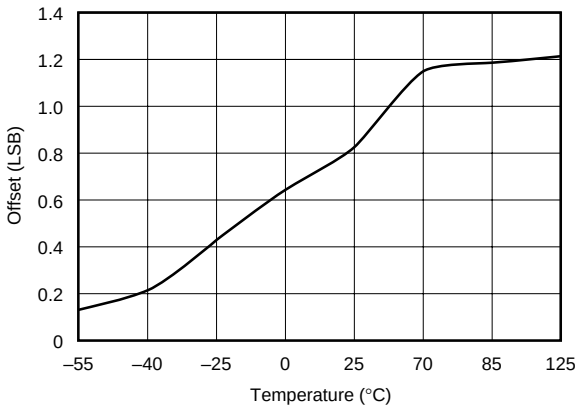
PIN NO	NAME	TYPE[1]	DESCRIPTION	PIN NO	NAME	TYPE[1]	DESCRIPTION
1	AN3N	AI	Auxiliary analog input channel 3, Negative Side	36	ADCLK	DI	Clock for the A/D converters. The nominal clock frequency is 1.25MHz.
2	AN3P	AI	Auxiliary analog input channel 3, Positive Side				
3	AN2N	AI	Auxiliary analog input channel 2, Negative Side	37	ADCONV	DI	Start signal for the A/D converter, active low. The first rising clock edge of ADCLK, when ADCONV is 0, starts the conversion.
4	AN2P	AI	Auxiliary analog input channel 2, Positive Side				
5	AN1N	AI	Auxiliary analog input channel 1, Negative Side	38	NPSH	DI	Sample/hold control for sampling the position sensor signals. If the value is 1, the signals are sampled, if it is 0 they are stored.
6	AN1P	AI	Auxiliary analog input channel 1, Positive Side				
7	NC	—	No Connection				
8	IWN	AI	Analog input of phase W current, Negative Side	39	ADIN	DI	Serial input signal for programming the D/A converter for setting the limit value of the current signals for the input voltage range of the A/D converters and for the input multiplexer of the A/D converters.
9	IWP	AI	Analog input of phase W current, Positive Side				
10	NC	—	No Connection				
11	IVN	AI	Analog input of phase V current, Negative Side				
12	IVP	AI	Analog input of phase V current, Positive Side	40	ADBUSY	DO	Conversion is executing, active low
13	NC	—	No Connection	41	DATACLK	—	Test pin, do not connect to in normal operation.
14	B1N	AI	Signal B analog input of position sensor 1, Negative Side	42	NC	—	No Connection
				43	NC	—	No Connection
15	B1P	AI	Signal B analog input of position sensor 1, Positive Side	44	NC	—	No Connection
				45	NC	—	No Connection
16	NC	—	No Connection	46	U_COMP	DO	Sign of phase U current signal (IUP, IUN). If the value is positive (IUP > IUN) U_COMP is 1, if the value is negative (IUP < IUN) U_COMP is 0.
17	B2N	AI	Signal B analog input of position sensor 2, Negative Side				
18	B2P	AI	Signal B analog input of position sensor 2, Positive Side	47	U_ILIM	DO	Over-current output of phase U, active low. If IUP-IUN is greater then the positive limiting value or less than the negative limiting value, U_ILIM becomes 0.
19	NC	—	No Connection				
20	NC	—	No Connection				
21	B_2	DO	Sign of signal B position sensor 2 (B2P, B2N). If the value is positive (B2P > B2N) B_2 is 1, if the value is negative (B2P < B2N) B_2 is 0.	48	A_1	DO	Sign of signal A position sensor 1 (A1P, A1N). If the value is positive (A1P > A1N) A_1 is 1, if the value is negative (A1P < A1N) A_1 is 0.
22	B_1	DO	Sign of signal B position sensor 1 (B1P, B1N). If the value is positive (B1P > B1N) B_1 is 1, if the value is negative (B1P < B1N) B_1 is 0.	49	A_2	DO	Sign of signal A position sensor 2 (A2P, A2N). If the value is positive (A2P > A2N) A_2 is 1, if the value is negative (A2P < A2N) A_2 is 0.
23	V_ILIM	DO	Over-current output of phase V, active low. If IVP-IVN is greater then the positive limiting value or less than the negative limiting value, U_ILIM becomes 0.	50	NC	—	No Connection
				51	NC	—	No Connection
				52	A2P	AI	Signal A analog input of position sensor 2, Negative Side
24	V_COMP	DO	Sign of phase V current signal (IVP, IVN). If the value is positive (IVP > IVN) V_COMP is 1, if the value is negative (IVP < IVN) V_COMP is 0.	53	A2N	AI	Signal A analog input of position sensor 2, Positive Side
				54	NC	—	No Connection
25	W_ILIM	DO	Over-current output of phase W, active low. If IWP-IWN is greater then the positive limiting value or less than the negative limiting value, U_ILIM becomes 0.	55	A1P	AI	Signal A analog input of position sensor 1, Positive Side
				56	A1N	AI	Signal A analog input of position sensor 1, Negative Side
26	W_COMP	DO	Sign of phase W current signal (IWP, IWN). If the value is positive (IWP > IWN) W_COMP is 1, if the value is negative (IWP < IWN) W_COMP is 0.	57	NC	—	No Connection
				58	IUP	AI	Analog input of phase U current, Positive Side
				59	IUN	AI	Analog input of phase U current, Negative Side
27	TP1	—	Test pin, do not connect to in normal operation.	60	NC	—	No Connection
28	TP2	—	Test pin, do not connect to in normal operation.	61	DAIN	AI	Input for setting the over-current value. Normally connected to DAOUT
29	UDP5V	P	Digital Supply Voltage, +5V				
30	DGND	P	Digital Supply Voltage, Ground	62	DAOUT	AO	Output of the D/A converter for programming the over-current limit. Output is programmable from 0V to +2.5V.
31	UDN5V	P	Digital Supply Voltage, –5V				
32	NC	—	No Connection				
33	ADOUT2	DO	Serial output signal of A/D converter 2. Rising clock edges of ADCLK outputs the bits of the A/D converter with MSB first.	63	REFOUT	AO	Output pin of the integrated reference source, nominal voltage 2.5V.
				64	REFIN	AI	Input pin for an external reference voltage.
34	ADOUT3	DO	Serial output signal of A/D converter 3. Rising clock edges of ADCLK outputs the bits of the A/D converter with MSB first.	65	REFGND	P	Ground pin of the reference source.
				66	UN5V	P	Analog Supply Voltage, –5V
				67	AGND	P	Analog Supply Voltage, Ground
35	ADOUT1	DO	Serial output signal of A/D converter 1. Rising clock edges of ADCLK outputs the bits of the A/D converter with MSB first.	68	UP5V	P	Analog Supply Voltage, +5V

NOTE: (1) AI is Analog Input, AO is Analog Output, DI is Digital Input, DO is Digital Output, P is Power Supply Connection.

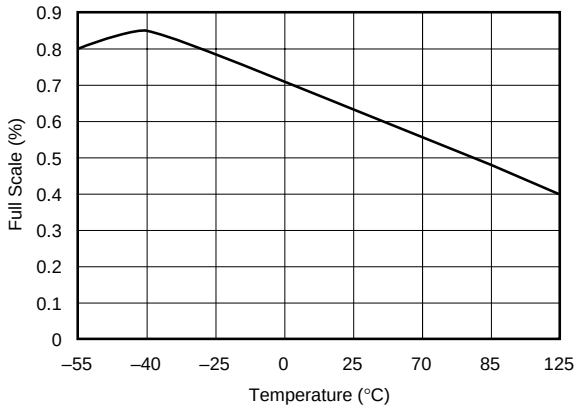
TYPICAL PERFORMANCE CURVES

At V_{ANA+} = +5V, V_{ANA-} = –5V, V_{DIG+} = +5V, V_{DIG-} = –5V and T_A = 25°C, using internal reference, f_{CLOCK} = 1.25MHz.

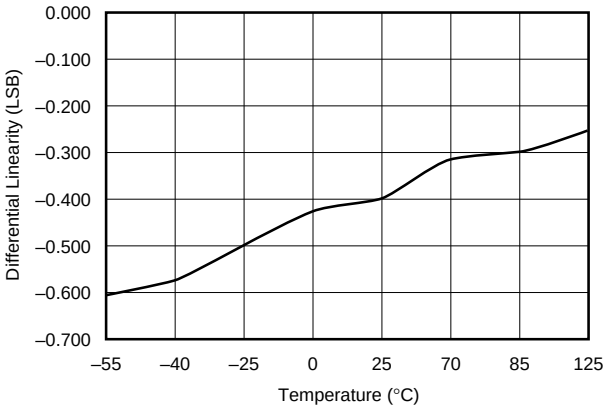
OFFSET vs TEMPERATURE



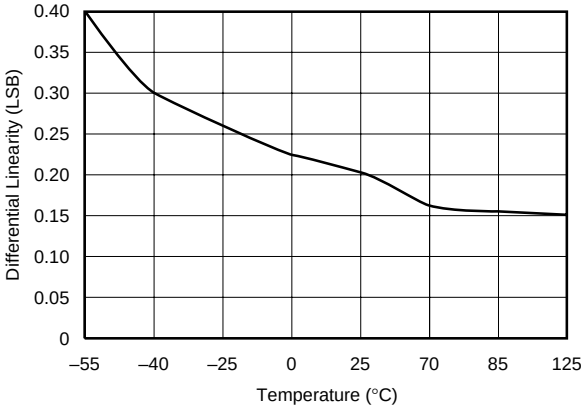
FULL SCALE vs TEMPERATURE



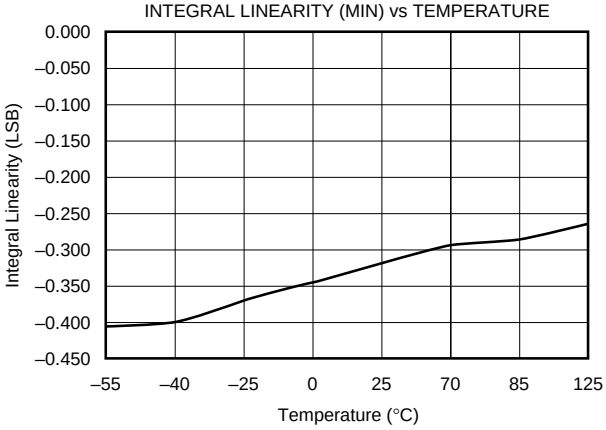
DIFFERENTIAL LINEARITY (MIN) vs TEMPERATURE



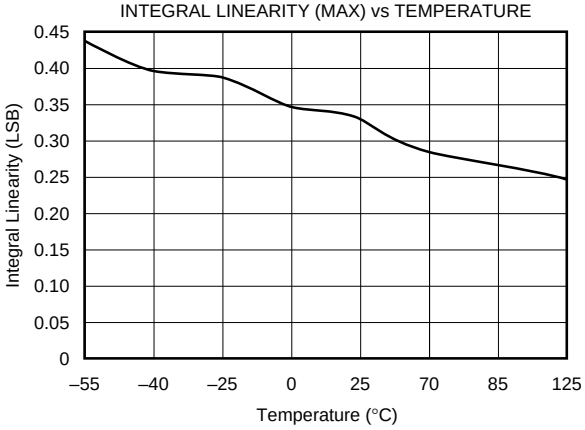
DIFFERENTIAL LINEARITY (MAX) vs TEMPERATURE



INTEGRAL LINEARITY (MIN) vs TEMPERATURE



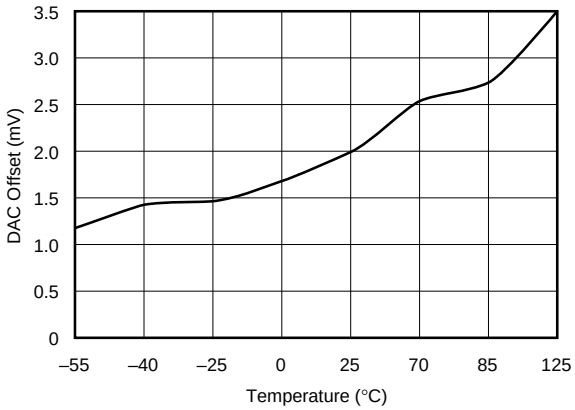
INTEGRAL LINEARITY (MAX) vs TEMPERATURE



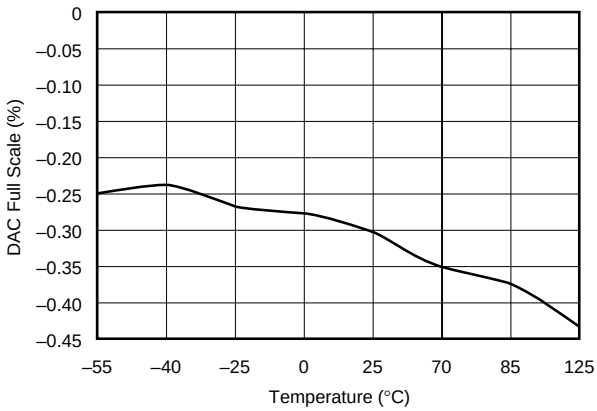
TYPICAL PERFORMANCE CURVES (Cont.)

At V_{ANA+} = +5V, V_{ANA-} = –5V, V_{DIG+} = +5V, V_{DIG-} = –5V and T_A = 25°C, using internal reference, f_{CLOCK} = 1.25MHz.

DAC OFFSET vs TEMPERATURE



DAC FULL SCALE vs TEMPERATURE



FUNCTIONAL DESCRIPTION

The VECAN01 is a triple 12-bit SAR A/D converter that operates from dual ±5V power supplies. The part contains three 12-bit successive approximation ADCs, multiplexer for 10 fully differential inputs, 5 differential input synchronized sample-and-hold amplifiers, plus two asynchronous sample-and-hold amplifier. It communicates over three synchronous SPI/SSI serial output and one input ports. The VECANA01 operates on external clock that also determines the output data rate (see Figure 2).

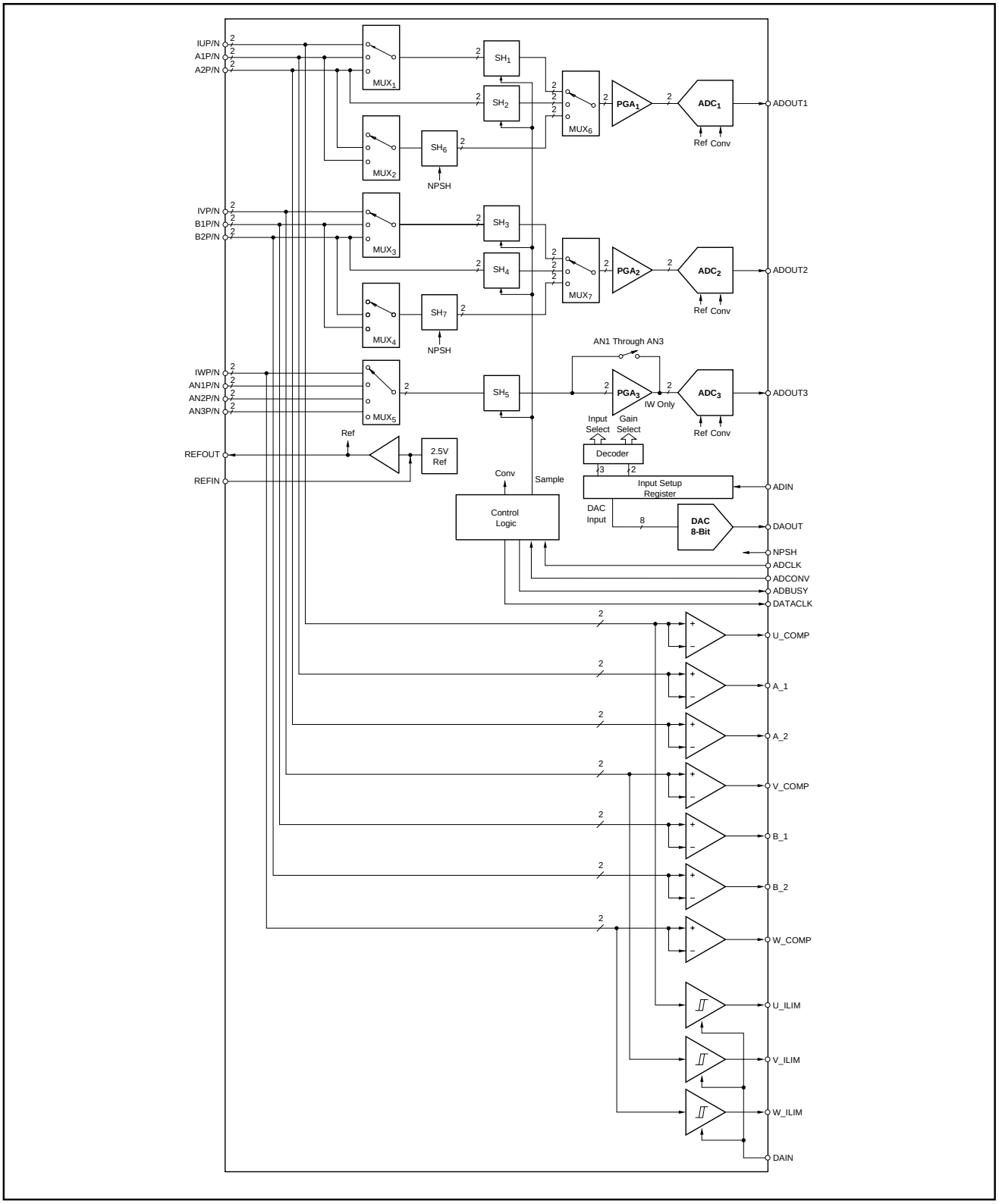


FIGURE 1. Functional Diagram.

MULTIPLEXERS

The VECANA01 has several input multiplexers that are used to select the desired analog inputs and connect the proper sample-and-hold outputs to the PGAs and A/D converters. A decoder receives its inputs from the Input Setup Register and drives the MUXs (see Table VII and Table VIII for information on selecting the input channel). The input multiplexers can take full differential or single-ended signals (see Figure 4 and Table III). The analog signals stay differential through the sample holds and the PGAs all the way to the inputs of the A/D converter. This provides the best possible noise rejection.

SAMPLE-AND-HOLD

The VECANA01 contains seven sample-and-hold amplifiers. Five of them (SH_1 through SH_5) sample simultaneously and have their sample-and-hold timing internally synchronized (the timing is shown in Figure 2). Three of the sample-and-holds (SH_1, SH_3, and SH_5) are connected to the input multiplexers so that they can provide simultaneous sampling for all of their channel inputs. In addition, SH_2 and SH_4 simultaneously sample the third input of their channel (A2 and B2, respectively). This is useful in motor control applications where A1 and B1 are the quadrature inputs for one position sensor, and A2 and B2 are the quadrature inputs for a second position sensor (see Figure 9). In that application, it is desirable to sample the quadrature inputs of a given position sensor at the same time (even though they are converted on successive conversion cycles) (see Table VII), so that their values are captured at the same shaft position. The VECANA01 also has the capability for limited asynchronous sampling. The sampling of SH_6 and SH_7 is controlled asynchronously by the control signal NPSH (see Table VII). This allows two inputs, each on Channel 1 and Channel 2 (see Table VIII) to be sampled asynchronously from the timing of the other sample holds. This can be useful in motor control applications where the two inputs for each channel need to be sampled asynchronously to a reference point.

ADCS AND PGAS

The VECANA01 contains three signal channels each with a 12-bit A/D converter output. The A/D converters operate synchronously and their serial outputs occur simultaneously (Table IX gives the analog input/digital output relationships). Programmable gain amplifiers precede the A/D converters (Table IX gives gain select information). For channels one and two, the PGAs are effective for all three analog inputs. For the third channel, only the IW input is gain changed by the PGA. Inputs AN1, AN2, and AN3 are connected to the A/D converter three at a fixed gain of 1.0V/V regardless of the gain select value.

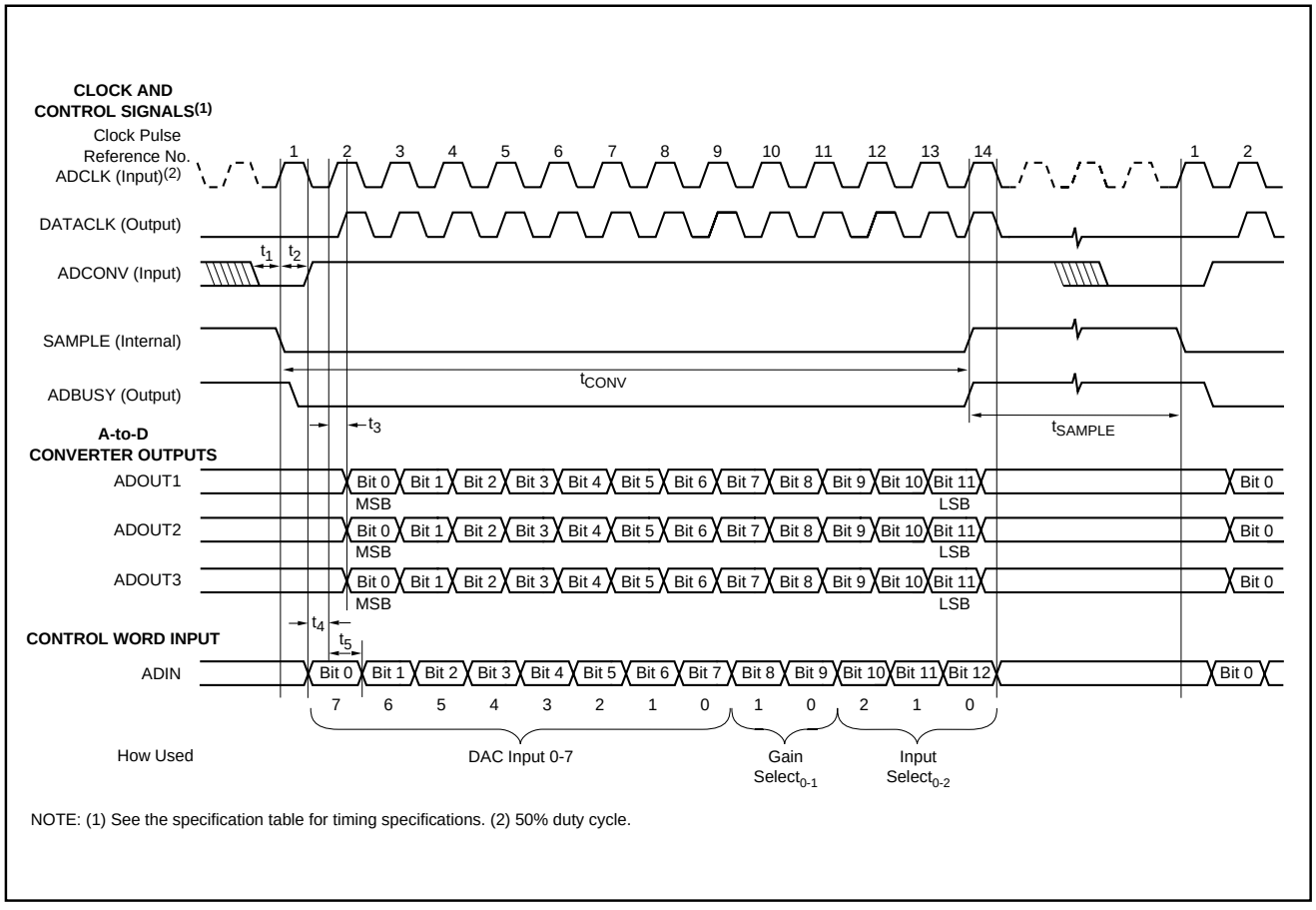


FIGURE 2. Timing Diagram.

VOLTAGE REFERENCE

The VECANA01 contains an internal 2.5V voltage reference. It is available externally through an output buffer amplifier. If it is desired to use an external reference, one may be connected at the REFIN pin. The output resistance of this pin for the external reference voltage is typically 7kΩ. This then overrides the internal 2.5V reference and is connected to the A/D converter. It is also available as a buffered output at the REFOUT pin.

The reference voltage shall be buffered by an external capacitor (approx. 2.2µF) on the REFIN pin and also on the REFOUT pin (see Figure 3), as close as possible to the pin.

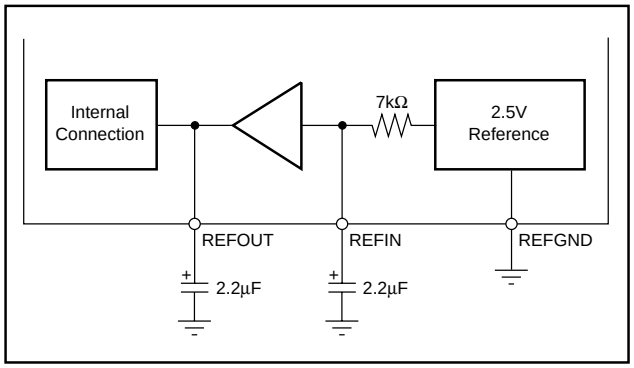


FIGURE 3. Reference Voltage Connection.

DIGITAL-TO-ANALOG CONVERTER

An 8-bit DAC provides 256 output voltage levels from 0V to 2.499V (see Table I for input/output relationships). The DAC is controlled by the DAC Input portion of the input setup word. The DAC Input portion of the word is strobed into the DAC at the end of the conversion cycle (14th CLK pulse in Figure 2).

DIGITAL INPUT DAC $INPUT_{0-7}$		ANALOG OUTPUT
HEX CODE	BINARY CODE	
00_H	0000 0000	0V
01_H	0000 0001	+0.0098V
•	•	•
•	•	•
•	•	•
FF_H	1111 1111	+2.499

TABLE I. DAC Input/Output Relationships.

DAC OUTPUT VOLTAGE

The value of the DAC output voltage is determined by the DAC Input portion of the ADIN word (bits 0 through 7, see Figure 2). The 8-bit DAC has 256 possible output steps from 0V to +2.499V. The value of 1LSB is 0.0098V.

OTHER DIGITAL INPUTS AND OUTPUTS

Sampling and conversion is controlled by the ADCONV and ADCLK input (see Figure 2). The VECANA01 is designed to operate from an external clock supplied at the ADCLK input. This allows the conversion to be synchronous with system timing so that transient noise effects can be minimized. The ADCLK signal may run continuously or may be supplied only during convert sequences. The ADBUSY and DATACLK signals are internally generated and are supplied to make interfaces with microprocessors easier (see Figures 2 and 9).

POWER-UP INITIALIZATION

When power is applied to the VECANA01, two conversion cycles are required for initialization before valid digital data is transmitted on the third cycle. The first conversion, after power is applied, is performed with indeterminate configuration values in the double buffer output of the Input Setup Register. The second conversion cycle loads the desired values into the register. The third conversion uses those values to perform proper conversions and output valid digital data from each of the A/D converters.

CLOCK POSITIONS(1)	DESCRIPTION	FUNCTIONS
2-9	DAC $Input_{0-7}$	Sets DAC Output Voltage
10-11	Gain $Select_{0-1}$	Sets PGA Gains
12-14	Input $Select_{0-2}$ Conditions	Determines Multiplexers
NOTE: (1) See Figure 2, "Clock Pulse Reference No."		

TABLE II. Description of Configurable Parameters.

CONFIGURABLE PARAMETERS

Configurable parameters are:

- PGA Gain
- Input Multiplexer and Sample-and-Hold Selection
- DAC Output Voltage

Configuration information for these parameters is contained in the ADIN word (see Figure 2). As one conversion is taking place, the configuration for the next conversion is being loaded into the buffered Input Setup Register via the ADIN word. Tables I, VII, VIII and X shows information regarding these parameters.

ANALOG-TO-DIGITAL CONVERTERS

ARCHITECTURE

The A/D converters are 12-bit, successive approximation types implemented with a switched capacitor circuitry.

CLOCK RATE

The clock for the A/D converter conversion is supplied externally at the ADCLK pin. Typical clock frequency for specified accuracy is 1.25MHz. This results in a complete conversion cycle (S/H acquisition and A/D conversion) of 10.4µs.

INPUT/OUTPUT

The VECANA01 is designed for bipolar input voltages and uses a binary two's complement digital output code. A programmable gain function is associated with each A/D converter. This changes the full-scale analog input range and the analog resolution of the converter. Details are shown in Table IX.

DIFFERENTIAL AND COMMON-MODE INPUT VOLTAGES

The VECANA01 is designed with full differential signal paths all the way from the multiplexer inputs through to the input of the A/D converters. This was done to provide superior high frequency noise rejection. As is common with most differential input semiconductor devices, there are compound restrictions on the combination of differential and common-mode input voltages. This matter is made slightly more complicated by the fact that most of the analog inputs are capable of being affected by the programmable gain function. The possible differential and single-ended configurations are shown in Figures 4a and 4b. The maximum differential and common-mode restrictions are shown in Table III.

GAIN SELECT CODE	0	1	2	3
Gain	5.0V/V	2.5V/V	1.25V/V	1.0V/V
Full Scale Range (V_D with V_{CM} = 0)	±0.5V	±1.0V	±2.0V	±2.5V
Largest Positive Common Mode Voltage, V_{CM}+	+2.7V	+2.4V	+1.9V	+1.6V
Largest Negative Common Mode Voltage, V_{CM}–	–2.7V	–2.4V	–1.9V	–1.6V

TABLE III. Differential and Common Mode Voltage Restrictions.

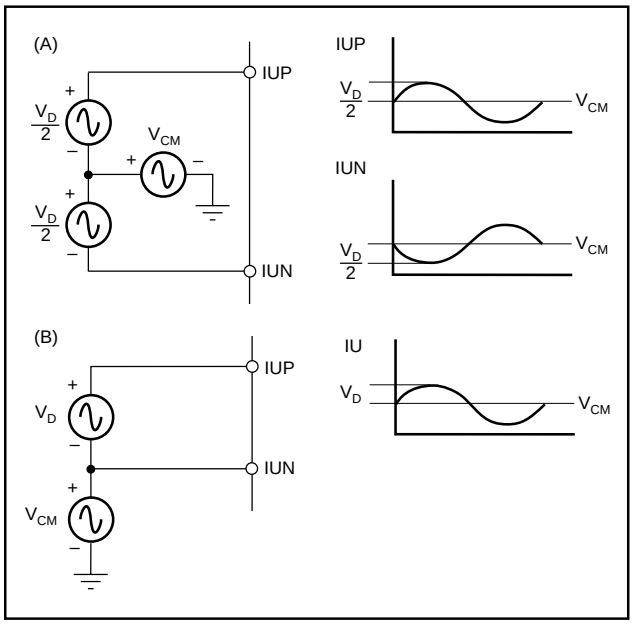


FIGURE 4. (a) Differential Signal Source. (b) Single-ended Input.

INPUT SETUP

As the A/D converters are converting and transmitting their serial digital data for one conversion cycle, a setup word is received to be used for the next conversion cycle. The 13-bit word is supplied at the ADIN pin (see Figure 1), and is stored in the buffered Input Setup Register. The Input Select and Gain Select portions of the word are decoded and determine the state of the multiplexers and PGAs (see CONFIGURABLE PARAMETERS section).

INPUT MULTIPLEXER AND SAMPLE HOLD SELECTION

The Input Select portion of the ADIN word (bits 10, 11 and 12) (see Figure 2) are decoded and determine the open/closed condition of the multiplexer switches. This in turn determines which input signals are connected to the sample and holds and which sample and holds are connected to the PGAs/ADCs.

SIGN OF THE INPUT SIGNALS

The VECANA01 contains seven comparators, which acquire the signals of the first seven input analog signals. The digital outputs of the sign comparators are the signals X_COMP. If the positive input value is greater than the negative input value, the X-COMP output becomes High (logic "1") or if the reverse, the X-COMP output is Low (logic "0"), (see Table IV).

IUP – IUN	U_COMP
A1P – A1N	A_1
A2P – A2P	A_2
IVP – IVN	V_COMP
B1P – B1N	B_1
B2P – B2N	B_2
IWP – IWN	W_COMP
> 0	1
< 0	0

TABLE IV. Input - Output Relation.

The typical hysteresis value of comparators U_COMP, V_COMP and W_COMP is 10mV. The typical hysteresis value of comparators A_1, A_2, B_1, and B_2 is 50mV. AC motor control applications will typically use 10mV hysteresis for phase current measurement and 50mV hysteresis for positioning sensor measurement.

OVER RANGE RECOGNITION

The VECANA01 also includes three window comparators for the three input signals IU, IV and IW. Each window comparator is composed of two comparators that are monitoring the input value on the positive range limit (U_{PLIM}) and negative range limit (U_{NLIM}). The output values of the window comparators are output via the pins U_ILIM, V_ILIM and W_ILIM. The two range limiting values are symmetrical to the zero point ($U_{NLIM} = -U_{PLIM}$) and are determined by pin

DAIN. See Figure 5 for graphical view of the over limit set function (typically used for setting the current protection value), The DAIN value will determine the fixed range. Normally this pin is connected to DAOUT (the DAC output). In order to be able to program the range value through the control value DAC Input word, the DAC Input is an 8-bit wide unsigned value (controls the digital-to-analog converter output voltage (DAOUT)). This D/A converter has an output voltage range of 0V to 2.5V (see Table I).

DAC INPUT	U_{PLIM}	U_{NLIM}
0H	0V	0V
1H	+0.0098V	–0.0098V
2H	+0.0195V	–0.0195V
0FEH	+2.4805V	–2.4805V
0FFH	+2.4902V	–2.4902V

TABLE V. Over-Current Limit as a Function DAC Input.

If the input voltage exceeds the positive range limit (IXP – IXN > U_{PLIM}) or it remains under the negative range (IXP – IXN < U_{NLIM}), then the corresponding window comparator output is Low (logic "0") (U_ILIM, V_ILIM, or W_ILIM). If the input value is within the limits, the comparator output is High (logic "1"). The input signal and output X_ILIM signals are shown in Table VI.

IUP – IUN IVP – IVN IWP – IWN	U_ILIM V_ILIM W_ILIM
(IXP - IXN) > U_{PLIM}	0
U_{PLIM} > (IXP - IXN) > U_{NLIM}	1
U_{NLIM} > (IXP - IXN)	0

TABLE VI. The Limiting Value as Function of DAC Input.

The input voltage range of the comparators is the same as the A/D converter when the Gain Select is 3. The typical value of the hysteresis of the comparators is 50mV. Figure 5 shows the Logic State of the U_COMP and U_ILIM outputs for the input signal IVP – IUN. The output resistance of the D/A converter is approximately 10kΩ. The output voltage, DAOUT should be buffered by a capacitor of approximately 100nF (see Figure 6) The resulting time constant is approximately 1ms and typical does not disturb most applications.

INPUT SIGNALS FOR PGAS/ADCS

Table VII shows the relationships between the value of Input $Select_{0-2}$ and the signals that are converted.

Input Select = 7H—Synchronously sample and convert input signals IU, IV, and IW.

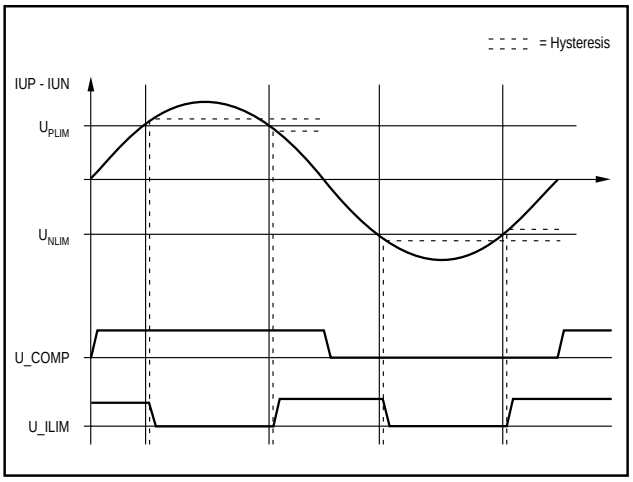


FIGURE 5. Acquisition of the Current Sign and of the Over-Current.

INPUT $SELECT_{0-2}$		ANALOG SIGNAL CONNECTED TO PGA_X/ADC_X		
HEX CODE	BINARY CODE	PGA_1/ADC_1	PGA_2/ADC_2	PGA_3/ADC_2
0_H	000	Undefined	Undefined	AN3
1_H	001	A_X via SH_6(1)	B_X via SH_7(1)	AN3
2_H	010	A_2 via SH_1	B_2 via SH_3	AN2
3_H	011	A_2 via SH_2	B_2 via SH_4	AN2
4_H	100	A1	B1	AN1
5_H	101	A1	B1	AN1
6_H	110	A1	B1	AN1
7_H	111	IU	IV	IW

NOTE: (1) See Table VIII for Operation.

TABLE VII. Input Controls for Synchronous Sample Holds.

Input Select = 4H, 5H, 6H—Synchronously sample and convert input signals A1, B1, and AN1. These codes also cause SH_2 and SH_4 to sample their inputs. Values 4_H, 5_H, 6_H have different effects on the inputs to SH_6 and SH_7 (see Table VIII).

INPUT $SELECT_{0-2}$		ANALOG SIGNAL CONNECTED TO	
HEX CODE	BINARY CODE	SH_6	SH_7
0_H	000	No Effect	No Effect
1_H	001	No Effect	No Effect
2_H	010	No Effect	No Effect
3_H	011	No Effect	No Effect
4_H	100	Open	Open
5_H	101	A1	B1
6_H	110	A2	B2
7_H	111	No Effect	No Effect

TABLE VIII. Input Controls for Asynchronous Sample Holds.

Input Select = 3H—Convert A2 via SH_2, B2 via SH_4, and AN2 (A2 and B2 are from the value sampled in a preceding conversion cycle with Input Select = 4_H, 5_H or 6_H).

Input Select = 2H —Convert A2 via SH_1, B2 via SH_3, and AN2.

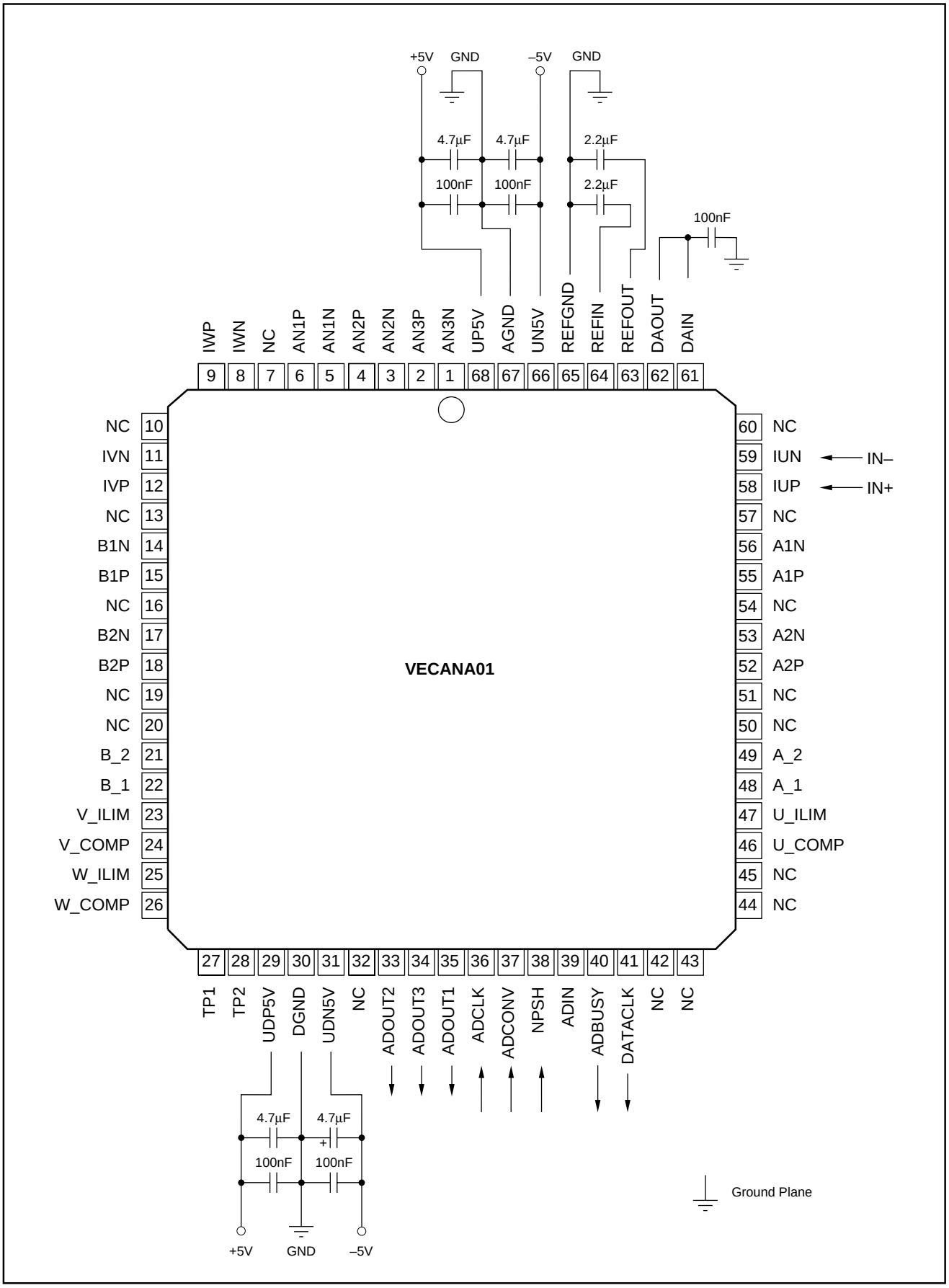


FIGURE 6. Basic Circuit Configuration.

DESCRIPTION	ANALOG INPUT				DIGITAL OUTPUT	
GAIN SELECT CODE	0	1	2	3		
GAIN	5V/V	2.5V/V	1.25V/V	1.0V/V	BINARY TWO'S COMPLIMENT FORMAT	
FULL SCALE RANGE	±0.5V	±1.0V	±2.0V	±2.5V	HEX CODE	BINARY CODE
+Full Scale (FS –1LSB)	+0.49976	+0.9995V	+1.999V	+2.499	$7FF_H$	0111 1111 1111
One Bit above Mid-Scale	+0.244mV	+0.488mV	+0.976mV	+1.22mV	001H	0000 0000 0001
Mid-Scale	0V	0V	0V	0V	000_H	0000 0000 0000
One Bit Below Mid-Scale	–0.244V	–0.488mV	–0.976mV	–1.22mV	FFF_H	1111 1111 1111
–Full Scale	–0.500V	–1.000V	–2.000V	–2.500V	800_H	1000 0000 0000

NOTE: The programmable gain function applies to all three input channels for ADC_1 and ADC_2. However, the programmable gain function only applies to the first input (IW) for ADC_3. The other three inputs (AN1, AN2, and AN3) are not affected by the GAIN SEL input. They operate at a fixed gain of 1V/V and thus have a fixed ±2.5V full scale input range.

TABLE IX. Analog Input - Digital Output Relationships.

Input Select = 1H—Input AN3 is converted by ADC_3. The output of the asynchronous sample holds, SH_6 and SH_7, are converted by PGA_1/ADC_1 and PGA_2/ADC_2, respectively. Note that the inputs to SH_6 and SH_7 are determined by previous Input Select values (see Table VIII). Thus, to properly convert the output of one of the asynchronous sample holds it is first necessary to choose its input with a previous conversion cycle. Also, the output of SH_6 or SH_7 will only be converted if NPSH goes low before the ADCONV command is received.

Input Select = 0 H—AN3 is converted by ADC_3. The inputs to PGA_1/ADC_1 and PGA_2/ADC_2 are undefined.

PGA GAIN

The PGA gain is determined by the Gain Select portion (bits 8 and 9) in the ADIN word (see Figure 2). There is one gain input that sets the same gain for all three PGAs. The gain values and allowable full-scale inputs are shown in Table X.

GAIN $SELECT_{0-1}$	GAIN SETTING	FULL SCALE INPUT
0_H	5.0V/V	±0.5V
1_H	2.5V/V	±1.0V
2_H	1.25V/V	±2.0V
3_H	1.0V/V	±2.5V

TABLE X. Gain Select Information.

For channels one and two the PGAs set the gain for all three analog inputs. For the third channel, only the IW input is gain changed by the PGA. Inputs AN1, AN2, and AN3 are connected to A/D converter three at a fixed gain of 1.0V/V regardless of the Gain Select value.

CONVERSIONS FROM THE ASYNCHRONOUS SAMPLE HOLDS

Decoding the Input Select value also determines which inputs are applied to the two asynchronously controlled sample holds (SH_6 and SH_7) (see Table VIII.) One of the three possible inputs is selected by the Input Select value being 4, 5, or 6. The "No Effect" states indicate that these values of Input Select have no effect on the multiplexers at the input of SH_6 and SH_7. When one of the "No Effect" values of Input Select is presented, the multiplexers will not be changed (i.e., their condition is determined by the last 4, 5, or 6 value of Input Select that existed prior to the "No Effect" state). Note that Input Select = 1_H presents the output of SH_6 and SH_7 to PGA_1/ADC_1 and PGA_2/ADC_2, respectively (see Table VII). Therefore, in order to properly convert the asynchronous sampled signals, it is first necessary to choose an input signal (Input Select equal 5 or 6 in Table VIII) with one load/convert cycle and then convert the sample hold output (Input Select = 4 in Table VII) in a following conversion cycle.

POWER SUPPLY

The VECANA01 requires an analog and digital supply voltage of ±5V. The substrate is connected to UP5V. The voltage difference between the analog and digital supply pin is not allowed to exceed a maximal value of 300mV. For this reason the circuit shown in Figure 7 is recommended for the power supply. The analog and digital power supplies are driven by a common source. Intermediate resistors provide for decoupling. Local current-limited voltage regulators generate the ±5V from the analog supply voltages $\pm U_B$. This guarantees a further noise reduction. The diodes are responsible for protecting the regulation and prevent polarity inversion. The zener diode protects against over-voltage possible from over-voltages to the analog inputs. Typical values for the resistors and capacitors are:

- $R_A \approx 3\Omega$
- $R_D \approx 3\Omega$
- $C_D \approx 22\mu F$
- $C_A \approx 22\mu F$
- $C_B \approx 100nF$
- $C_R \approx 2.2\mu F$

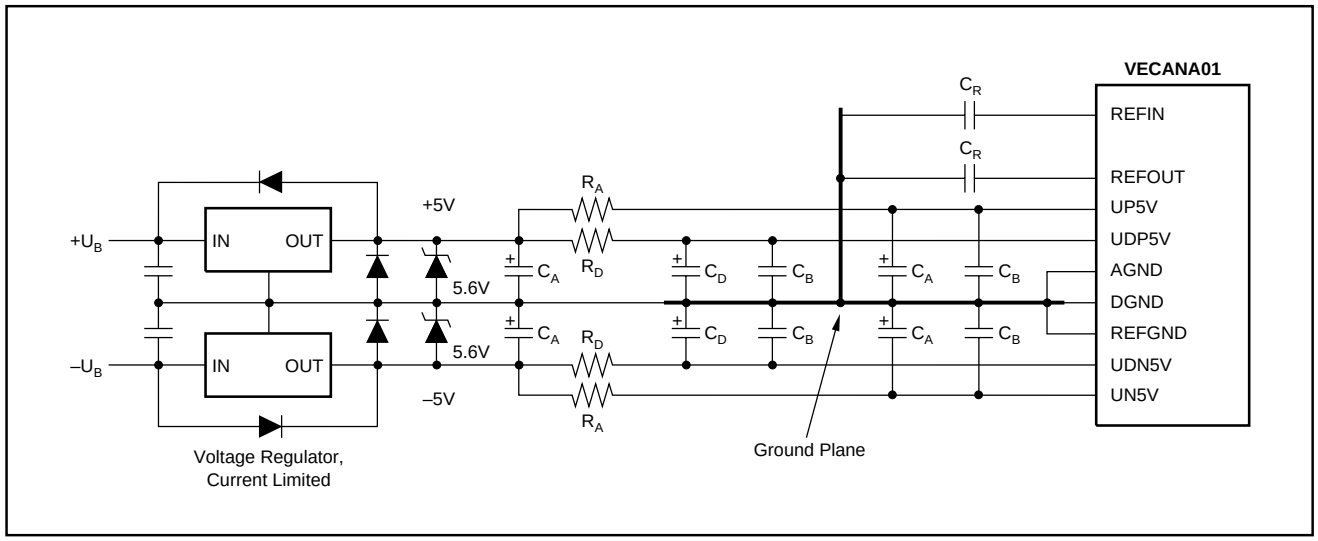


FIGURE 7. Power Supply of VECANA01.

CONNECTION BETWEEN VECANA01 AND DSP

The interface between the VECANA01 and dSMC101 comprises the control signals for the A/D converters (ADCLK, ADCONV, ADIN, ADOUT1-3, NPSH, ADBUSY and DATACLK) and the comparator signals (X_COMP and X_ILIM). The signal levels and the driver capacity of the two chips are compatible. In order to avoid noise injection of the digital power supply into the analog VECANA01 chip, it is recommended to damp all digital lines with an intermediate resistor of approximately 100Ω as near as possible to the analog chip.

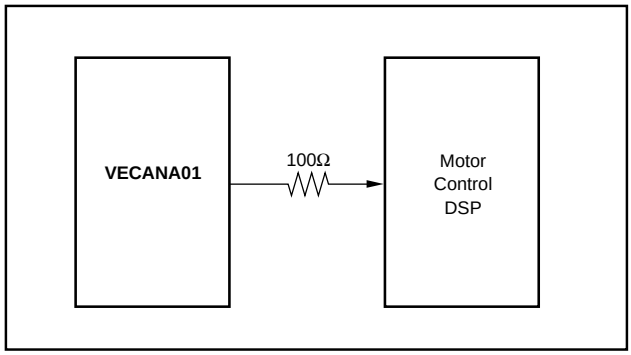


FIGURE 8. Damping of All Digital Lines.

SICAN dSMC101 INTERFACE

The internal logic of the VECANA01 is designed for easy control and data interface with DSPs. Figure 9 shows the interface for loading the input control word from the DSP data bus into the serial input of the VECANA01.

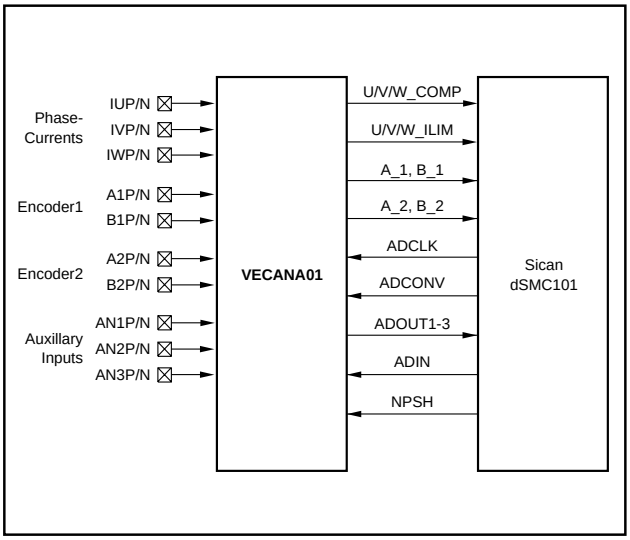


FIGURE 9. DSP Interface for Sican dSMC101.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
VECANA01	NRND	PLCC	FN	68	20	Green (RoHS & no Sb/Br)	Call TI	Level-3-260C-168 HR
VECANA01G3	ACTIVE	PLCC	FN	68	20	Green (RoHS & no Sb/Br)	Call TI	Level-3-260C-168 HR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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